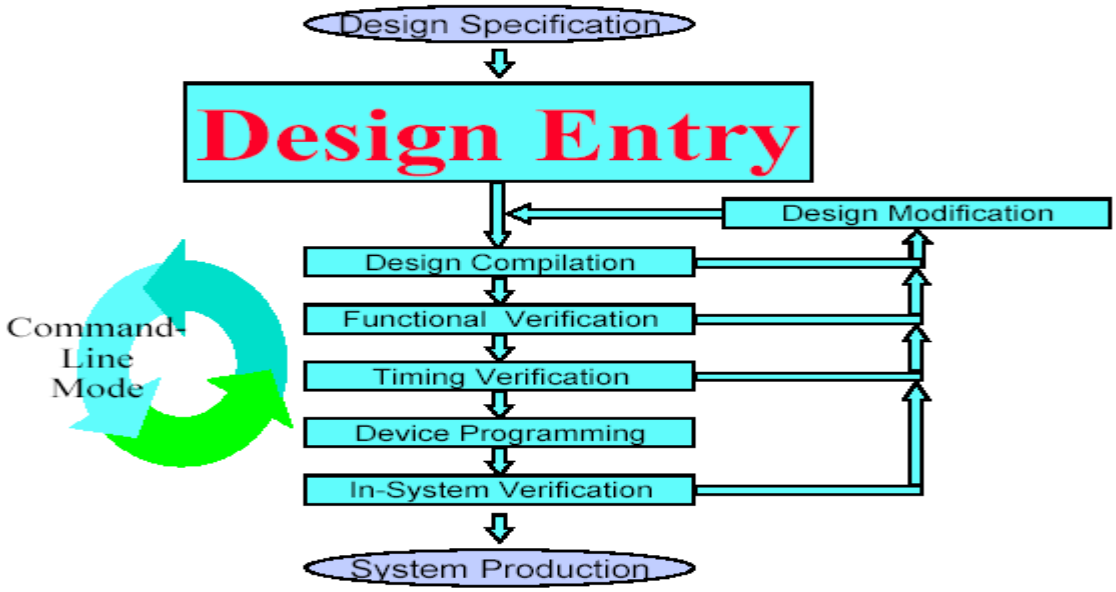
Kuwait University
Electrical Engineering Department
MAX+ PLUS II

Done by Eng. Ahmad Haitham

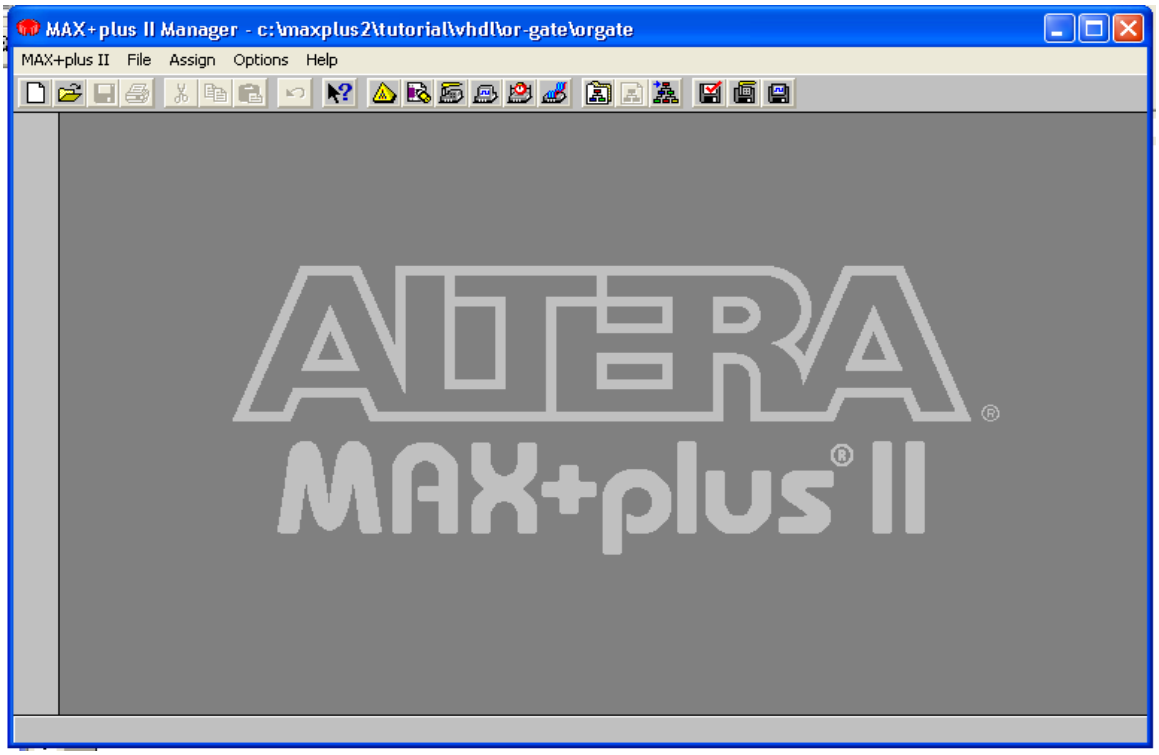
A-Design Methodology:



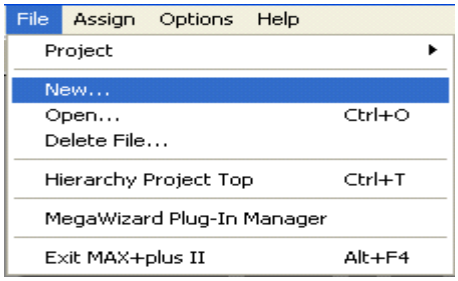
B-To start MAX+PLUS II

1-Double click on the MAX+PLUS II icon 

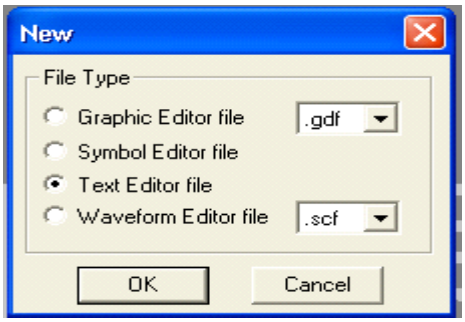
The software will shows the following window.



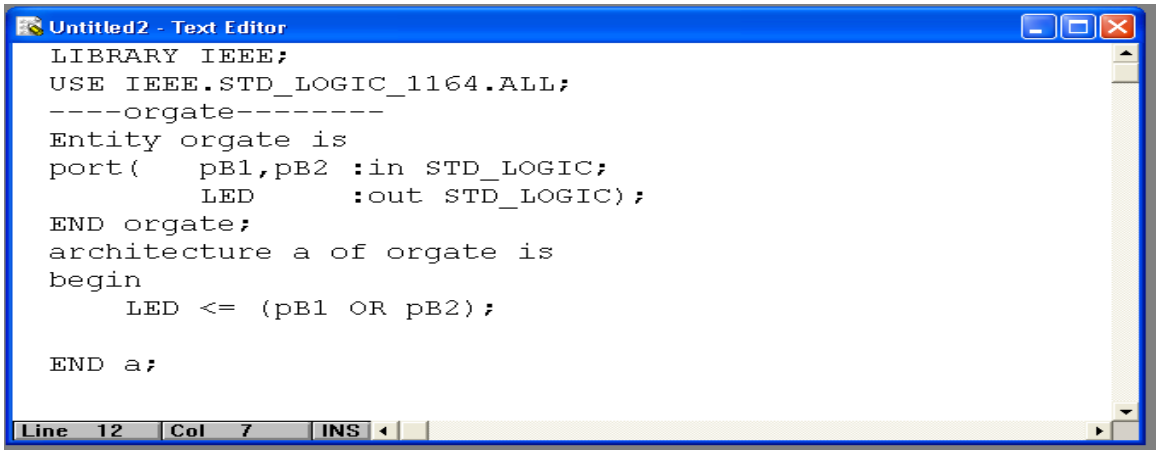
2- Select **File** ⇒ **New.**



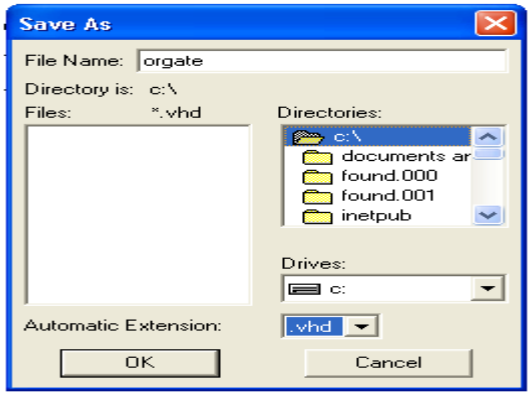
3- Select **Text Editor File.**



4- In the new empty window write the VHDL input file**.**

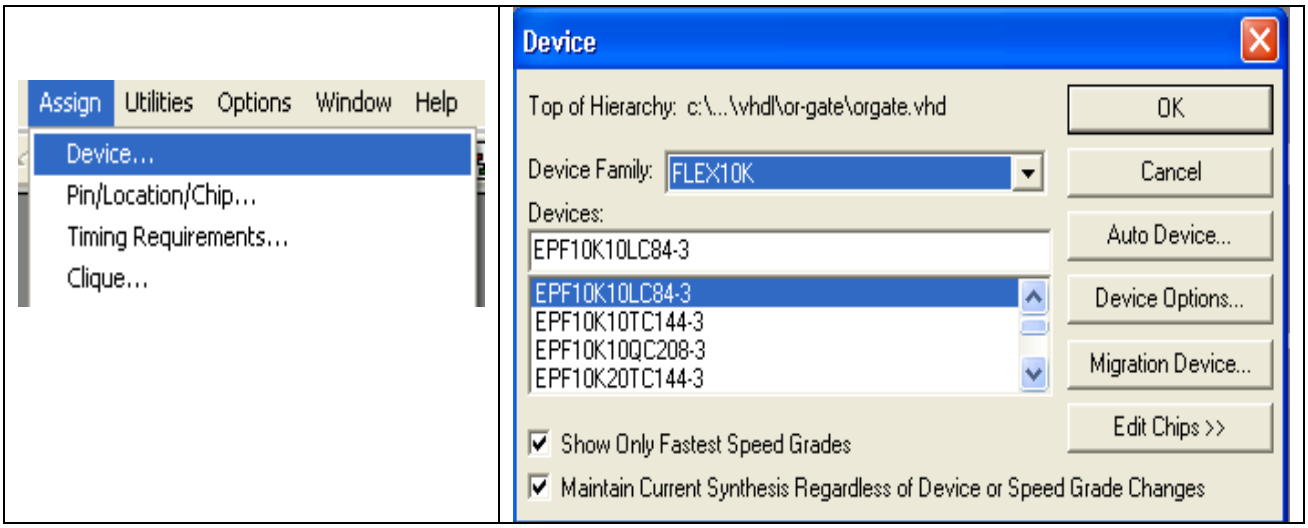


5- Save the File as Vhd ,Select **File** ⇒ **Save As.**

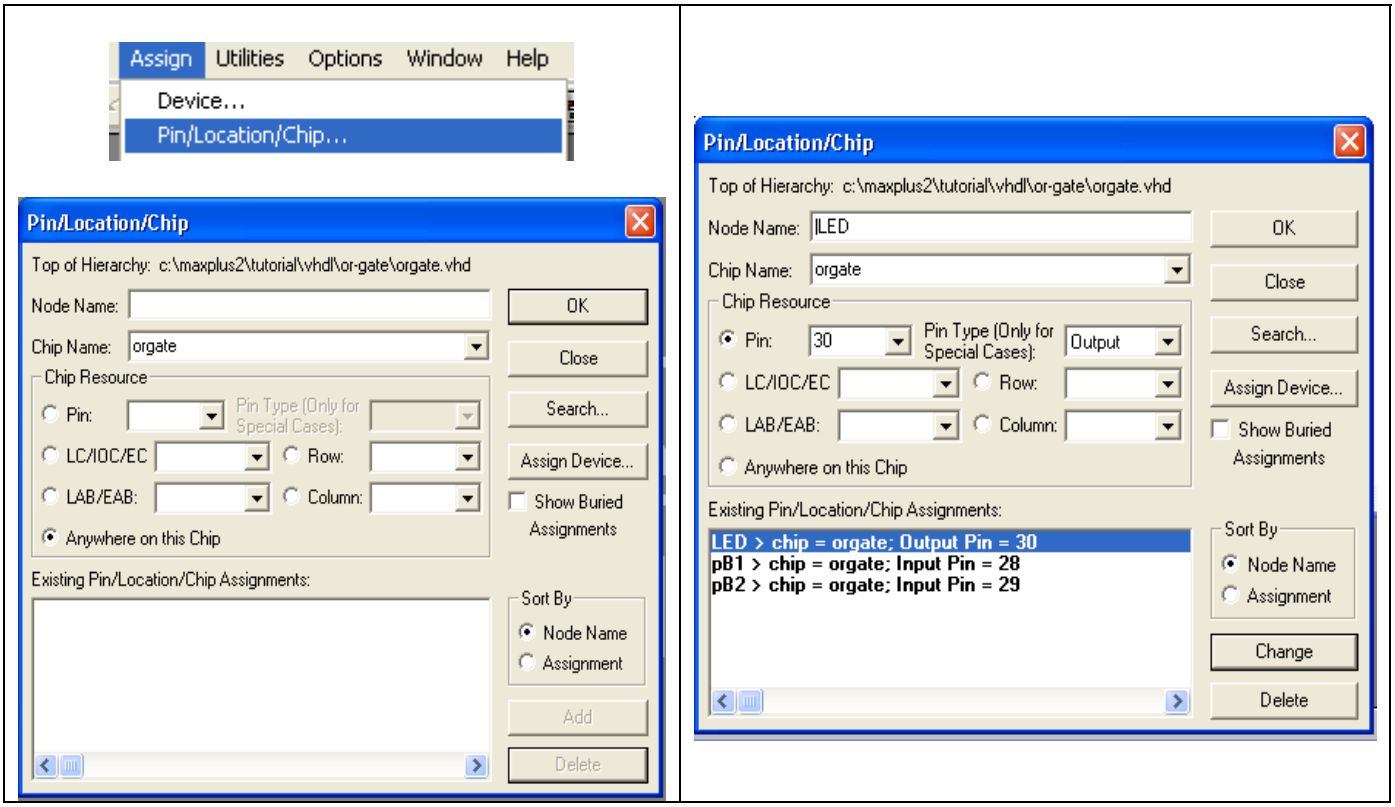


6- Select **Assign ⇒ Device.**

To assign the chip that will be used to configure the design. Here FLEX10K is assigned with the chip number EPF10K10LC84-3 that is written on the chip.



7- Select **Assign ⇒ Pin/Location/Chip.**



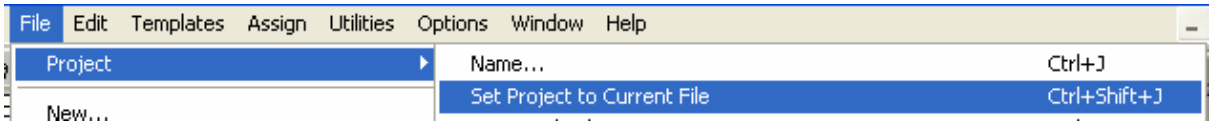
Click on Search, then Click on List**,** all input and outputs names will appear. Select one, return to the previous window. Next to **Pin**, select the down arrow and scroll down to select pin 28 or just enter 28 in the space provided. Repeat this process assigning pin 29 to PB2 and pin 30 to **LED.**

Device	Pin Number Connections
PB1	28
PB2	29
LED Decimal Point On the left Seven-Segment Display	30

Device and pin information is stored in the project's *.acf file. Caution: Be sure to use unique names for different pins..

8- Set project to Current File

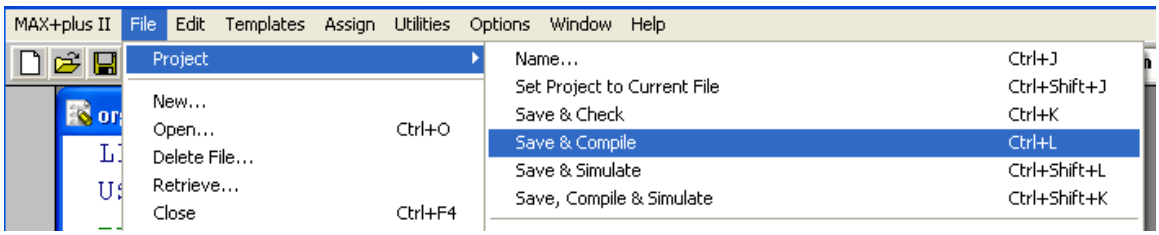
Select **File Project ⇒ Set Project to Current File.**



9- Compiling the Design

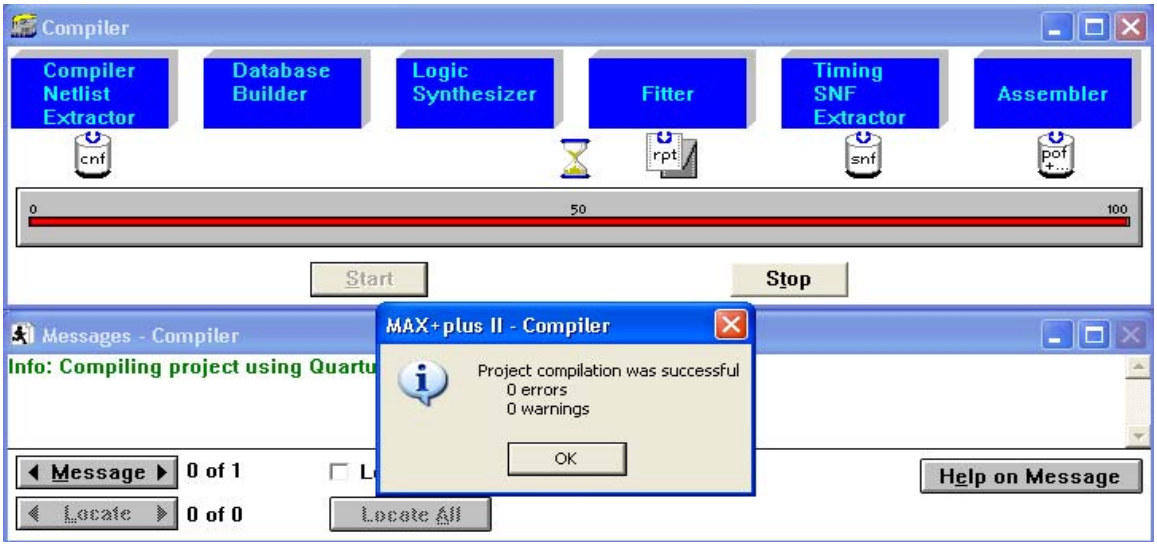
Compiling your design checks for syntax errors, synthesizers the logic design produces timing information for simulation, fits the design for the selected CPLD, and generates the file required to download the program. After any changes are made to the design files or pin assignments, the project should always be re-compiled prior to simulation or downloading.

Compile by selecting **File ⇒ Project ⇒ Save and Compile.**
A window with the modular compiler, will monitor compiling, warnings and errors.



10- Checking for Compile Warnings and Errors

The project should compile with **0 errors**. If the message states, "Project Compilation," then you have not made an error. Warnings about forcing pin assignment can be ignored.



Examining the Report File

View the orgate.rpt file by double clicking on the icon below the filter block in the compile window. After compilation, a *.rpt file is created that contains information on device utilization, pin assignments, and a copy of the netlist. After reviewing this file, close it and return to the circuit with

File ⇒ Close.

11- Simulation of the Design

For complex design, the design would normally be simulated prior to downloading to a CPLD. Although the OR example is straightforward, we will take you through the steps to illustrate the simulation of the circuit.

Set Up the Simulation Traces

Choose **File ⇒ New,** select Waveform Editor File, and then from the popup window click OK. The waveform window should be displayed. Select **Node ⇒ Enter Node from SNF.** (A SNF is a Simulator Netlist File. It contains timing information about your circuit that allows the software to produce a timing diagram output display.) Click on the **LIST** button. PB1, PB2 and LED should appear as trace value in the window. Then click on the center => button and click on **OK.**

General Test Vectors for Simulation

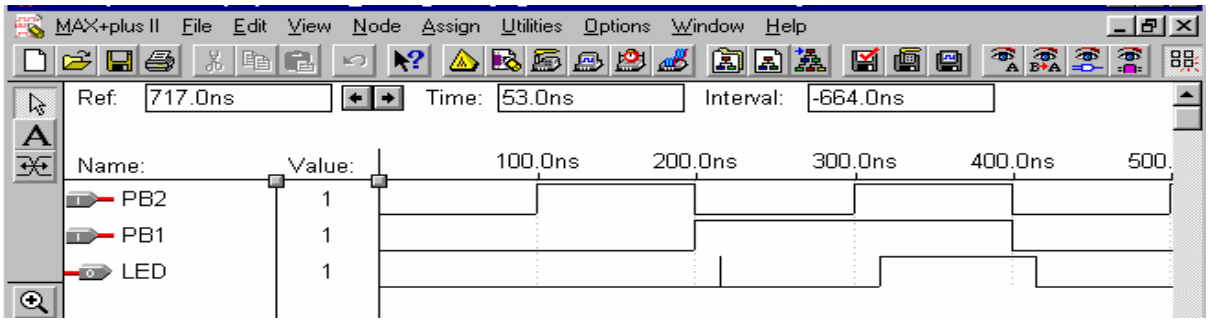
A simulation requires external input data or “stimulus” data to test the circuit. Since the PB1 and PB2 signals have not been set, the simulator sets them to a default of zero. The ‘X’ on the LED trace indicates that the simulator has not been run. (If the simulator *has* been run and you still get an ‘X’, then the simulator was unable to determine the output condition.)

Right click on **PB1**. The PB1 trace will be highlighted. Select **Overwrite ⇒ Count Value …** and click **OK**. An alternating pattern of Highs and Lows should appear in the

PB1 trace. Next, select **View ⇒ Time Range …** and set the **From** and **To** range to 0.0ns and 500.0ns respectively.
Right click on **PB2**. Select **Overwrite ⇒ Count Value …,** and change the entry for **Multiplied By** from **1** to **2**, and click **OK**. **PB2** should now be an alternating pattern of ones and zeros but at half the frequency of PB1. (Other useful options in the **Overwrite** menu will generate a clock and set a signal High or Low. It is also possible to highlight a portion of a signal trace with the mouse and set it High or Low manually.)

12- Performing the Simulation with Your Timing Diagram

Select **File ⇒ Project ⇒ Save, Compile, and Simulate**. Click **OK**. The simulation should run and the waveform for LED should now appear as seen in figure x.6. Note that the simulation includes the actual device timing delays through the device and that it takes around 20ns (ns = 10^{-9} sec.) for the output to reflect the new inputs. Verify that the LED output is Low only when eitherPB1 OR PB2 inputs are Low.

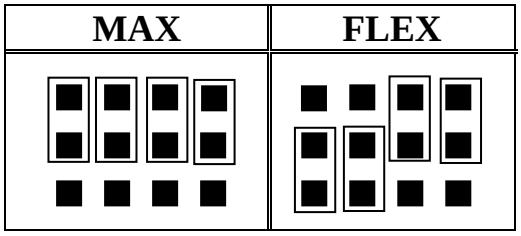


13- Downloading Your Design to the UP 1 or UP 1X Board

Hooking UP1 the UP2 Board to the Computer

Plug the Byteblaster* cable into the UP 1 or UP 2 board and attach the other end to the parallel port on a PC. If you have not done so already, make sure that the PC's BIOS setting for the printer port is ECP or EPP mode. Using a 9V AC to DC wall transformer or another 7 to 9V DC power source, attach power to the DC power connector (DC_IN) located on the upper left-hand corner of the UP 1 board. When properly powered, one of the green LEDs on the board should light up.

Verify that the device jumpers are set for the FLEX chip as shown below. The locations of the pushbuttons.



Preparing for Downloading

After checking to make sure that the cables and jumpers are hooked up properly, you are ready to download the compiled circuit to the UP 1 board. Select **MAX+PLUS II ⇒ Programmer.** From **Options ⇒ Hardware ⇒ Setup,** select the proper output port: normally **LPT1.** (If a window comes up that displays, **"No Hardware",** use the pull-down to change **"No Hardware"** to **"Byteblaster".** If this still doesn't correct the problem, then there is something else wrong with the setup.

To install the ByteBlasterMV driver file for Windows XP, follow these steps:

1. Choose Control Panel (Windows Start menu).
2. Click the Switch to Classic View link.
3. In the Control Panel window, double-click Add Hardware and choose Next. The Add Hardware wizard appears.
4. In the first page of the Add Hardware wizard, select Yes, I have already connected the hardware, and choose Next.
5. Select Install the hardware that I manually select from a list (Advanced) and choose Next.
6. Select Sound, video and game controllers and choose Next.
7. Select Have disk.
8. Specify the full directory path to the **\maxplus2\drivers\win2000** directory with Browse (...) and choose OK.
9. In the Digital Signature Not Found page, choose Yes. A software installation warning appears.
10. Choose Continue Anyway.
11. Select Altera ByteBlaster and choose Next. A hardware installation warning appears.
12. Choose Continue Anyway.
13. Choose Finish.
14. When prompted to restart your computer, choose Yes.

JTAG Setup

THIS NEEDS TO BE DONE EACH TIME THE DESIGN FILENAMESIS CHANGED.

Select **JTAG ⇒ Multi-device JTAG chain** so that a checkmark appears to the left of the option. Next select **JTAG ⇒ Multi-device JTAG setup.** Hit the **Select programming File** button and select **orgate.sof.** Click **OK**, then click the **ADD** button and the new filename should move into the list in the inner window. Delete any other entries that may be in this window.
Select the **Detect JTAG Chain Info** button. The system should respond with "JTAG chain information confirmed by hardware check". If not, double check cables, power, jumpers, and make sure you have the correct file name and chip listed in the inner window. Click **OK** to exit the **JTAG Multi-device Setup** window.

Final Setup to Download

The **configure** button in the programming window should now be highlighted. Click on the **configure** button to download to the board. Just a few seconds are required to download. If download is successful, a window with **Configuration Complete** is displayed - click **OK.** (If the **configure** button is not highlighted, try **Option ⇒ Hardware Setup** from the pull-down window. confirm the port settings and click **OK.** Also confirm that the JTAG setup dialog information is correct. If you still have problems confirm that the printer port BIOS settings ESP or EPP mode).